AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) A pulse width modulation controlling circuit for a power supply comprising:

a processor means for generating a time-length signal comprising a first and second portion;

a counting means for receiving said first portion of said time-length signal and counting in discrete coarse steps to a predetermined number determined by said first portion of said time-length signal for providing a coarse adjusted signal, said counting means outputting said coarse adjusted signal;

a delay means operatively connected to said counting means for receiving said coarse adjusted signal; and

a selection means coupled to said delay means for receiving said second portion of said time-length signal and for selecting a predetermined discrete delay period in said delay means, for creating discrete time steps, whereby said power supply is capable of providing a plurality of repeatable output pulses.

2. (Original) The apparatus of claim 1, wherein said counting means is a digital counting means.

3. (Original) The apparatus of claim 2, wherein said digital counting means comprises a programmable logic device.

4. (Original) The apparatus of claim 3, herein said counting means comprises an oscillator means operating at a predetermined frequency.

5. (Original) The apparatus of claim 4, wherein said oscillator means oscillates at approximately 125 MHz.

6. (Original) The apparatus of claim 1, wherein said delay means delays in increments of 0.25 nanoseconds.

7. (Original) The apparatus of claim 1, wherein said delay means is an analog delay means.

8. (Original) The apparatus of claim 1, wherein said delay means is a digital delay means.

9. (Original) The apparatus of claim 7, wherein said delay means comprises a plurality of inductors and capacitors connected in a series-parallel configuration.

10. (Original) The apparatus of claim 1, wherein said selection means is a digital selection means.

11. (Original) The apparatus of claim 9, wherein said selection means is a multiplexor.

12. (Original) The apparatus of claim 1, wherein said processor means operates at a first voltage, and said counting means, delay means, and selection means operates at a second voltage.

13. (Original) The apparatus of claim 12, wherein said apparatus further comprises a first and second transforming means, a power converter means, and a power conditioning means, wherein an output of said processing means is coupled to said first transforming means for transforming said output of said processing means at said first voltage to said second voltage, and an output of said second selection means is coupled to said power converting means, said second transformer means, and said power conditioning means.

14. (Original) The apparatus of claim 1, wherein said counting means, said delay means and said selection means are disposed in said processing means.

15. (Original) A method for controlling a switchmode power supply comprising:

generating a time-length signal;

transmitting a first portion of said time-length signal to a counting means, and a second portion of said time-length signal to a selection means;

counting to a number based on said first portion of said time-length signal received by said counting means;

outputting a coarse adjusted signal from said counting means after counting to said predetermined number;

selecting a delay from a delay means based on said second portion of said time-length signal received by said selection means;

delaying said coarse adjusted signal a predetermined length of time based on said selected delay in said delay means; and

outputting an output signal after said predetermined delay.

16. (Original) A pulse width modulation controlling circuit for a power supply comprising:

a processor means for generating a time-length signal comprising a first and second portion;

a first selection means for receiving said first portion of said time-length signal, and for selecting one of a plurality of counting means, wherein said selected one of said plurality of counting means receives said first portiono f said time-length signal and counts in discrete coarse steps to a predetermined number determined by said first portion of said time-length signal for providing a coarse adjusted signal, said selected one of said plurality of counting means outputting said coarse adjusted signal;

17. (Original) The apparatus of claim 16, wherein each one of said plurality of counting means counts at a unique, predetermined rate.

18. (Original) The apparatus of claim 16, wherein said plurality of counting means are digital counting means.

19. (Original) The apparatus of claim 16, wherein said each one of said plurality of counting means comprises a programmable logic device.

20. (Original) The apparatus of claim 16, wherein said counting means comprises an oscillator means operating at a predetermined frequency.

21. (Original) The apparatus of claim 16, wherein said delay means is an analog delay means.

22. (Original) The apparatus of claim 16, wherein said delay means is a digital delay means.

23. (Original) The apparatus of claim 21, wherein said delay means comprises a plurality of inductor and capacitors connected in a series-parallel configuration.

24. (Original) The apparatus of claim 16, wherein said first selection means is a digital selection means.

25. (Original) The apparatus of claim 24, wherein said first selection means is a multiplexor.

26. (Original) The apparatus of claim 16, wherein said second selection means is a digital selection means.

27. (Original) The apparatus of claim 26, wherein said second selection means is a multiplexor.

28. (Original) The apparatus of claim 16, where in said processor means operates at a first voltage, and said first selection means, said plurality of counting means, delay means, and second selection means operates at a second voltage.

29. (Original) The apparatus of claim 28, wherein said apparatus further comprises a first and second transforming means, a power converter means, and a power conditioning means, wherein an output of said processing means is coupled to said first transforming means for transforming said output of said processing means at said first voltage to said second voltage, and an output of said second selection means is coupled to said power converting means, said second transformer means, and said power conditioning means.

30. (Original) The apparatus of claim 16, wherein said counting means, said delay means and said selection means are disposed in said processing means.

31. (Currently Amended) A pulse width modulation controlling circuit for a power supply comprising:

a processor ~~means~~ for generating a time-length signal comprising a first portion and second portion;

a counting ~~means~~ circuit for receiving said first portion of said time-length signal and counting in discrete coarse steps to a predetermined number determined by said first portion of said time-length signal for providing a coarse adjusted signal, said counting ~~means~~ circuit outputting said coarse adjusted signal;

a delay selection ~~means~~ circuit for receiving said second portion of said time-length signal;

a plurality of delay ~~means~~ circuits operatively connected to said plurality of counting means for receiving said coarse adjusted signal; and

a plurality of second selector ~~means~~ circuits wherein said delay selection ~~means~~ circuit selects one of said plurality of second selector ~~means~~ circuits, and wherein a second selector ~~means~~ circuit is coupled to each one of said plurality of delay ~~means~~ circuits, said selected one of said plurality of second selector ~~means~~ circuits for selecting a predetermined discrete delay period in one of said plurality of delay ~~means~~ circuits, for creating discrete time steps, whereby said power supply is capable of providing a plurality of repeatable output pulses.

32. (Currently Amended) The apparatus of claim 31, wherein said counting ~~means~~ circuit is a digital ~~counting means~~ circuit.

33. (Currently Amended) The apparatus of claim 32, wherein said digital counting ~~means~~ circuit comprises a programmable logic device.

34. (Currently Amended) The apparatus of claim 33, wherein said counting ~~means~~ circuit comprises an oscillator ~~means~~ operating at a predetermined frequency.

35. (Currently Amended) The apparatus of claim 34, wherein said oscillator ~~means~~ oscillates at approximately 125 MHz.

36. (Currently Amended) The apparatus of claim 31, wherein said delay ~~means~~ circuit delays in increments of 0.25 nanoseconds.

37. (Currently Amended) The apparatus of claim 31, wherein said delay selection ~~means~~ circuit is a digital ~~delay selection means~~ circuit.

38. (Currently Amended) The apparatus of claim 37, wherein said delay selection ~~means~~ circuit is a multiplexor.

39. (Currently Amended) The apparatus of claim 31, wherein said plurality of second selector ~~means~~ circuits are digital ~~selector means~~ circuits.

40. (Currently Amended) The apparatus of claim 39, wherein said plurality of second selector ~~means~~ circuits are multiplexors.

41. (Currently Amended) The apparatus of claim 31, wherein each one of said plurality of delay ~~means~~ circuits delays said coarse adjusted signal in unique, predetermined increments.

42. (Currently Amended) The apparatus of claim 31, wherein each one of said plurality of delay ~~means~~ circuits is an analog ~~delay means~~ circuit.

43. (Currently Amended) The apparatus of claim 42, wherein each one of said plurality of delay ~~means~~ circuits comprises a plurality of inductor and capacitors connected in a series-parallel configuration.

44. (Currently Amended) The apparatus of claim 31, wherein each one of said plurality of delay ~~means~~ circuits is a digital ~~delay means~~ circuit.

45. (Currently Amended) The apparatus of claim 31, wherein said processor ~~means~~ circuit operates at a first voltage, and said counting ~~means~~ circuit, delay selection ~~means~~ circuit, plurality of delay ~~means~~ circuits, plurality of second and said selector ~~means~~ circuits, operates at a second voltage.

46. (Currently Amended) The apparatus of claim 45, wherein said apparatus further comprises a first and second transforming ~~means~~ circuit, a power converter ~~means~~ circuit, and a power conditioning ~~means~~ circuit, wherein an output of said processing ~~means~~ circuit is coupled to said first transforming ~~means~~ circuit for

transforming said output of said processing ~~means~~ circuit at said first voltage to said second voltage, and an output of each one of said plurality of second selector ~~means~~ circuits, said selection ~~means~~ circuit is coupled to power converting ~~means~~ circuit, said second transformer ~~means~~ circuit, and said power conditioning ~~means~~ circuit.

47. (Currently Amended) The apparatus of claim 31, wherein said counting ~~means~~ circuit, said delay ~~means~~ circuit and said selection ~~means~~ circuit are disposed in said ~~processing means~~ processor.

48. (Currently Amended) A pulse width modulation controlling circuit for a power supply comprising:

a processor ~~means~~ for generating a time-length signal comprising a first and second portion;

a first ~~selection means~~ selector for receiving said first portion of said time-length signal, and for selecting one of a plurality of ~~counting means~~ counters, wherein said selected one of said plurality of ~~counting means~~ counters receives said first portion of said time-length signal and counts in discrete coarse steps to a predetermined number determined by said first portion of said time-length signal for providing a coarse adjusted signal, said selected one of said plurality of counting means outputting said coarse adjusted signal;

a delay ~~selection means~~ selector for receiving said second portion of said time-length signal;

a plurality of delay ~~means~~ elements operatively connected to said plurality of ~~counting means~~ counters for receiving said coarse adjusted signal; and

a plurality of second ~~selector means~~ selectors, wherein said delay ~~selection means~~ selector selects one of said plurality of second ~~selector means~~ selectors, and wherein a second selector ~~means~~ is coupled to each one of said plurality of delay ~~means~~ elements, said selected one of said plurality of second ~~selector means~~ selectors for selecting a predetermined discrete delay period in one of said plurality of delay ~~means~~ elements, for creating discrete time steps, whereby said power supply is capable of providing a plurality of repeatable output pulses.

49. (Currently Amended) The apparatus of claim 48, wherein each one of said plurality of counting ~~means~~ counters counts at a unique, predetermined rate.

50. (Currently Amended) The apparatus of claim 48, wherein said plurality of ~~counting means~~ counters are digital ~~counting means~~ counters.

51. (Currently Amended) The apparatus of claim 48, wherein said first ~~selection means~~ is a digital ~~selection means~~ selector.

52. (Currently Amended) The apparatus of claim 48, wherein said first ~~selection means~~ selector is a multiplexor.

53. (Currently Amended) The apparatus of claim 48, wherein said delay ~~selection means~~ element is a digital delay ~~selection means~~ element.

54. (Currently Amended) The apparatus of claim 53, wherein said delay ~~selection means~~ selectors is a multiplexor.

55. (Currently Amended) The apparatus of claim 48, wherein said plurality of second ~~selector means~~ selectors are digital ~~selector means~~ selectors.

56. (Currently Amended) The apparatus of claim 55, wherein said plurality of second ~~selector means~~ selectors are multiplexors.

57. (Currently Amended) The apparatus of claim 48, wherein each one of said plurality of delay ~~means~~ elements delays said coarse adjusted signal in unique, predetermined increments.

58. (Currently Amended) The apparatus of claim 48, wherein each one of said plurality of delay ~~means~~ elements is an analog ~~delay means~~ element.

59. (Currently Amended) The apparatus of claim 58, wherein each one of said plurality of delay ~~means~~ elements comprises a plurality of inductor and capacitors connected in a series-parallel configuration.

60. (Currently Amended) The apparatus of claim 48, wherein each one of said plurality of delay ~~means~~ elements is a digital delay ~~means~~ element.

61. (Currently Amended) The apparatus of claim 48, wherein said ~~processing means~~ processor operates at a first voltage, and said first ~~selection means~~ selector, plurality of ~~counting means~~ counters, delay ~~selection means~~ selectors, plurality of delay ~~means~~ elements and said plurality of second ~~selector means~~ selectors operates at a second voltage.

62. (Currently Amended) The apparatus of claim 61, wherein said apparatus further comprises a first and second ~~transforming means~~ transform circuit, a power converter ~~means~~, and a power ~~conditioning means~~ conditioner, wherein an output of said ~~processing means~~ processor is coupled to said first ~~transforming means~~ transform circuit for transforming said output of said ~~processing means~~ processor at said first voltage to said second voltage, and an output of each one of said plurality of second ~~selector means~~ selectors is coupled to said power ~~converting means~~ converter, said second ~~transformer means~~ transform circuit, and said power ~~conditioning means~~ conditioner.

63. (Currently Amended) The apparatus of claim 48, wherein said ~~counting means~~ counter, said delay ~~means~~ element and said ~~selection means~~ selector are disposed in said ~~processing means~~ processor.

64. (Currently Amended) A method for controlling a switchmode power supply in a plasma chamber comprising:

generating a time-length signal;

transmitting a first portion of said time-length signal to a counting ~~means~~ circuit, and a second portion of said time-length signal to a selection ~~means~~ circuit;

counting to a number based on said first portion of said time-length signal received by said ~~counting means~~ counting circuit;

outputting a coarse adjusted signal from said counting ~~means~~ circuit after counting to said predetermined number;

selecting a delay from a delay ~~means~~ circuit based on said second portion of said time-length signal received by said selection ~~means~~ circuit;

delaying said coarse adjusted signal a predetermined length of time based on said selected delay in said delay ~~means~~ circuit; and

outputting an output signal to said power supply in said plasma chamber after said predetermined delay.

65. (Currently Amended) The ~~apparatus~~ method of claim 64, wherein said counting ~~means~~ circuit is a digital ~~counting means~~ circuit.

66. (Currently Amended) The ~~apparatus~~ method of claim 65, wherein said digital counting ~~means~~ circuit comprises a programmable logic device.

67. (Currently Amended) The ~~apparatus~~ method of claim 66, wherein said counting ~~means~~ circuit comprises an oscillator means operating at a predetermined frequency.

68. (Currently Amended) The ~~apparatus~~ method of claim 67, wherein said oscillator ~~means~~ oscillates at approximately 125 MHz.

69. (Currently Amended) The ~~apparatus~~ method of claim 64, wherein said delay ~~means~~ circuit delays in increments of 0.25 nanoseconds.

70. (Currently Amended) The ~~apparatus~~ method of claim 64, wherein said delay ~~means~~ circuit is an analog ~~delay means~~ circuit.

71. (Currently Amended) The ~~apparatus~~ method of claim 64, wherein said delay ~~means~~ circuit is a digital ~~delay means~~ circuit.

72. (Currently Amended) The ~~apparatus~~ method of claim 70, wherein said delay ~~means~~ circuit comprises a plurality of inductors and capacitors connected in a series-parallel configuration.

73. (Currently Amended) The ~~apparatus~~ method of claim 64, wherein said selection ~~means~~ circuit is a digital selection ~~means~~ circuit.

74. (Currently Amended) The ~~apparatus~~ method of claim 64, wherein said selection ~~means~~ circuit is a multiplexor.

75. (Currently Amended) The ~~apparatus~~ method of claim 64, wherein said processor ~~means~~ operates at a first voltage, and said counting ~~means~~ circuit, delay ~~means~~ circuit, and selection ~~means~~ circuit operates at a second voltage.

76. (Currently Amended) The ~~apparatus~~ method of claim 75, wherein said apparatus further comprises a first and second ~~transforming means~~ transform circuit, a power converter ~~means~~, and a power ~~conditioning means~~ conditioner, wherein an output of said ~~processing means~~ processor is coupled to said first ~~transforming means~~ transform circuit for transforming said output of said ~~processing means~~ processor at said first voltage to said second voltage, and an output of said second selection ~~means~~ circuit is coupled to said power ~~converting means~~ converter, said second transformer means is coupled to said power converting means, said second ~~transformer mean~~ transform circuit, and said power ~~conditioning means~~ conditioner.

77. (Currently Amended) The ~~apparatus~~ method of claim 64, wherein said counting ~~means~~ circuit, said delay ~~means~~ circuit and said selection ~~means~~ circuit is disposed in said ~~processing means~~ processor.

78. (Currently Amended) The ~~process~~ method of claim 64, wherein the step of generating a time-length signal further comprises generating said time-length signal in a processor ~~means~~.

79. (Currently Amended) The ~~process~~ method of claim 64, wherein said counting ~~means~~ circuit is a digital ~~counting means~~ circuit.